REMARKS

This Amendment is filed in response to the Office Action dated January 27, 2005, which has a shortened statutory period set to expire April 27, 2005.

Applicants Address Concerns Regarding The Declaration And Power Of Attorney Form

Applicants appreciate the Examiner's close attention to detail in this case. On April 16, 2001, Applicants submitted a Response To Notice of Missing Parts and a Declaration signed by Tom Williams. A copy of this correspondence is attached.

Applicants Address Objection To Figure 2

Applicants have amended Figure 2 to delete reference to the Memory1 Mask Memory (without reference number). Based on this deletion, Applicants request reconsideration and withdrawal of the objection to Figure 2.

Applicants' New Abstract

Applicants submit that the new Abstract provided herein is less than 150 words, and therefore request entry of the new Abstract.

Applicants Overcome Objections To Claim 7

Applicants have amended Claim 7 to correct a typographical error. Based on this correction, Applicants request reconsideration and withdrawal of the objection to Claim 7.

Applicants Overcome 112 Rejections Of Claims 10 And 17

Applicants have amended Claims 10 and 17 to correct for antecedent basis. Based on these amendments, Applicants request

reconsideration and withdrawal of the rejections of Claims 10 and 17.

Claims 7-13 and 17-20 Are Patentable Over The Cited References

Claims 1-6 are cancelled, thereby rendering the rejection of those claims moot.

Applicant respectfully traverses the rejection of Claims 7-13. Specifically, Claim 7 recites:

> An integrated circuit testing system comprising:
> a) an integrated circuit tester comprising:
> a1) a first memory for storing therein a mask vector for characterizing corresponding test vector data, said mask vector comprising a plurality of bit positions wherein a first bit value indicates that said corresponding test vector data is deterministic and wherein a second bit value indicates that said corresponding test vector data is pseudo random; and
> a2) a second memory for storing therein deterministic test vector data, said first and second memory coupled to a port;
> b) an integrated circuit device under test (DUT) comprising:
> b1) a circuit block to be tested;
> b2) a random number generator for generating a reproducible sequence of pseudo random bits based on a seed number; and
> b3) a selector circuit coupled to said port and for generating a test vector for application to said circuit block, said selector circuit for selecting bits as between said random number generator and said second memory based on said mask vector, said selector circuit having an output coupled to said circuit block.

Applicants respectfully submit that Jarwala fails to disclose or suggest the recited IC tester and IC DUT. As taught

by Applicants in reference to Figure 3, which illustrates an exemplary implementation:

> The system of Figure 3 acts to reduce the throughput of the data flowing from the tester 14' to the DUT 16'. The embodiment of Figure 3 reduces the tester throughput to the DUT 16' by incorporating the LFSR circuit 230 on the DUT 16' itself. A configurability mechanism for sending data from the tester 14' or the compressed data source on the DUT 16' can be built-in. The control of the source of test data to the design would lie in the hands of the control logic 250 of the tester 14'. The embodiment of Figure 3 also offers an increase in performance. Specifically, this configuration allows for the possibility of obtaining and applying the data portion that is generated on the DUT 16' at a faster rate than that could be achieved from a low cost tester.

Specification, page 20, lines 4-13.

In contrast, Jarwala fails to teach that the device under test (DUT) includes the random number generator and the selector circuit. Therefore, Jarwala cannot achieve the tester throughput and the performance provided by Applicants' recited testing system. Because Jarwala fails to disclose or suggest the recited testing system, Applicants request reconsideration and withdrawal of the rejection of Claim 7.

Claims 8-13 depend from Claim 7 and therefore are patentable for at least the reasons presented for Claim 7. Moreover, with respect to Claims 11 and 12, Lesmeister fails to remedy the deficiencies of Jarwala. Based on all of the above reasons, Applicants request reconsideration and withdrawal of the rejection of Claims 8-13.

Claims 14-16 are cancelled, thereby rendering the rejection of those claims moot.

Claim 17 now recites:

> A method for testing an integrated circuit

comprising the steps of:

a) retrieving a mask vector from a first memory, said mask vector for characterizing corresponding test vector data, said mask vector comprising a plurality of bit positions wherein a first bit value indicates that said corresponding test vector data is deterministic and wherein a second bit value indicates that said corresponding test vector data is pseudo random;

b) retrieving deterministic test vector data from a second memory;

c) initializing a random number generator with a seed number and thereafter generating a reproducible sequence of pseudo random bits based on said seed number;

d) generating an output test vector for application to a circuit block of said integrated circuit, said step d) comprising the step of selecting bits as between said random number generator and said second memory based on said mask vector

e) applying said output test vector to said circuit block;

f) obtaining an output generated by said circuit block in response to said output test vector; and

g) supplying said output generated by said circuit block to an input of a stage of said random number generator.

Applicants respectfully submit that Jarwala fails to disclose or suggest the recited step of supplying the output generated by the circuit block to an input of a stage of the random number generator (i.e. step g)). As taught by Applicants in reference to Figure 4B, which illustrates an exemplary implementation:

> Figure 4B illustrates another embodiment of the LFSR circuit 230b which 5 can interleave output values from the DUT 16 using OR gates 320-322. By interleaving the output values (e.g., over output lines 330-332) into the LFSR 230b, the effective "randomness" of the result is increased. This also increases error detection because an error on the output lines 330-332 will

> generate an improper input test pattern which will likely lead to another departure from the expected result on the output, etc. This increases the likelihood that the error is detected by the verification circuitry 240 (Figure 2, Figure 3). The output lines 330-332 originate from the output of the DUT 16. The value of line 330 is ORed into the output of the first stage 310. The value of line 331 is ORed into the output of the second stage 311. The value of line 332 is ORed into the output of the third stage 312. It is appreciated that any number of stages can be used in accordance with this embodiment of the present invention.
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> Specification, page 22, lines 4-16.

In contrast, Jarwala fails to teach supplying the output generated by the circuit block to an input of a stage of the random number generator. Therefore, Jarwala cannot achieve the effective "randomness" provided by Applicants' recited method. Because Jarwala fails to disclose or suggest the recited method, Applicants request reconsideration and withdrawal of the rejection of Claim 17.

Claims 18-20, as amended, now depend from Claim 17 and therefore are patentable for at least the reasons presented for Claim 17. Moreover, with respect to Claim 18, Lesmeister fails to remedy the deficiencies of Jarwala. Based on all of the above reasons, Applicants request reconsideration and withdrawal of the rejection of Claims 18-20.

CONCLUSION

Claims 7-13 and 17-20 are pending in the present Application. Reconsideration and allowance of these claims is respectfully requested.

If there are any questions, please telephone the undersigned at 408-451-5907 to expedite prosecution of this case.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

4/30/2005 Rebecca A. Baumann
Date Signature: Rebecca A. Baumann